UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,923	06/27/2003	Hiromitsu Miyamoto	MAE 288	3860

23995 7590 02/23/2006

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,923	MIYAMOTO, HIROMITSU	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 June 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/6/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on April 06, 2004 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The drawings were received on 6/27/03 are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu U.S. Patent No. 5,727,035 in view of Baba et al. U.S. Patent No. 6,856,658.

As per claims 1 and 9, Hiramatsu substantially teaches the claimed method and synchronization error detection circuit in which A synchronization device has a first section for generating a predetermined signal. A second section is operative for detecting a correlation between a received signal and the predetermined signal generated by the first section. A third section is operative for generating a predetermined correlation reference. A fourth section is operative for calculating an error between the correlation detected by the second section and the predetermined correlation reference generated by the third section. A fifth section is operative for comparing the error calculated by the fourth section with a predetermined threshold value to detect synchronization timing. (Abstract, Figure 1) Not disclosed by Hiramatsu is the detection of transition of the pluses.

However in an analogous art, Baba et al. teach the clock signal selecting circuit selects the selected clock signal from the N clock signals based on an average falling edge phase data, and outputs the selected clock signal to the output switching circuit. The switching circuit passes the N sampled data signals in response to the first selection signal. The phase comparing circuit compares

the selected clock signal and each of the N sampled data signals in phase to output post-comparison data signals. The average falling edge phase determining circuit determines an average falling edge phase from the N sampled data signals to output the average falling edge phase data to the clock signal selecting circuit. The average rising edge phase determining circuit determines an average rising edge phase from the N sampled data signals to output an average rising edge phase data. The duty detecting circuit detects a duty of each of the N sampled data signals to produce duty data. The identifying circuit determines a data selection phase based on the average rising edge phase data and the duty data for the N sampled data signals. Also, the identifying circuit selects one from the post-comparison data signals which has a phase near to the data selection phase, and outputs the selected post-comparison data signal as a selection data signal. The re-timing circuit carries out a re-timing operation to the selection data signal based on the selected clock signal to output to the output switching circuit. (Column 5 lines 16-45)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the synchronization detection circuit and method of Hiramatsu with the pulse detecting circuit of Baba et al. This would have been obvious and one would have been motivate to make this combination as suggested by Hiramatsu (column 1 lines 8-14) for accurate recovery of transmitted information.

As per claims 2 and 10, Baba et al. teach that each of the plurality of internal circuits may include a clock signal selecting circuit, a switching circuit, a

phase comparing circuit, an average falling edge phase determining section, an average rising edge phase determining section, a duty detecting circuit, an identifying circuit and a re-timing circuit. The clock signal selecting circuit selects the selected clock signal from the N clock signals based on an average falling edge phase data, and outputs the selected clock signal to the output switching circuit. The switching circuit passes the N sampled data signals in response to the first selection signal. The phase comparing circuit compares the selected clock signal and each of the N sampled data signals in phase to output post-comparison data signals. The average falling edge phase determining circuit determines an average falling edge phase from the N sampled data signals to output the average falling edge phase data to the clock signal selecting circuit. The average rising edge phase determining circuit determines an average rising edge phase from the N sampled data signals to output an average rising edge phase data. The duty detecting circuit detects a duty of each of the N sampled data signals to produce duty data. The identifying circuit determines a data selection phase based on the average rising edge phase data and the duty data for the N sampled data signals. Also, the identifying circuit selects one from the post-comparison data signals which has a phase near to the data selection phase, and outputs the selected post-comparison data signal as a selection data signal. The re-timing circuit carries out a re-timing operation to the selection data signal based on the selected clock signal to output to the output switching circuit. (Column 4 lines 17-49)

As per claims 3 and 11, the synchronization error detector includes a decision circuit that compares a difference between said successive average values with a predetermined threshold value, a synchronization error being detected when the difference exceeds the predetermined threshold value. (Hiramatsu column 2 lines 9-11, and Baba et al. column 10 lines 33-44 and column 11 lines 4-17)

As per claims 4 and 12, Baba et al. teach that the average rising edge phase calculating circuit is composed of a calculating circuit as a combination circuit and a storage circuit of a flip-flop circuit. The average rising edge phase calculating circuit is supplied with the reset signal, the falling edge data, and the selected clock signal. The reset signal indicates the head of the burst data signal. The calculating circuit of the average falling edge phase calculating circuit calculates the current average rising edge phase data from the rising edge data, the past average falling edge phase data and the number of past rising edge data in response to the selected clock signal. The calculating circuit increments the number of past falling edge data by "1". Also, the calculating circuit outputs the current average falling edge phase data to the clock signal selecting circuit as the clock selection signal and the storage circuit. The storage circuit of the average falling edge phase calculating circuit latches the current average falling edge phase data in response to the selected clock signal. Then, the storage circuit outputs the latched average falling edge phase data to the calculating circuit and the rising edge detecting circuit as the past average falling edge phase data and to the falling edge detecting circuit as current average falling

edge phase data. The calculating circuit and the storage circuit are reset in response to the reset signal. (Column 14 lines 3-27)

As per claims 5 and 13, although by definition, a difference between consecutive transitions would in fact be a pulse width, by calculating the average, as in the previous claims rejected above) one would inherently have calculated the pulse width.

As per claims 6, 7, 14 and 15, the synchronization error detector includes a decision circuit that compares a difference between said successive average values with a predetermined threshold value, a synchronization error being detected when the difference exceeds the predetermined threshold value. (Hiramatsu column 2 lines 9-11, and Baba et al. column 10 lines 33-44 and column 11 lines 4-17)

As per claims 8 and 16-18, the examiner would like to point out that the prior art is replete with references having a retransmission request generator for sending a retransmission request to a transmitting source (also having and entire subclass 714/748 dedicated to this retransmission. The same logic may also be used with respect to disabling error detection and/or correction of data. As the examiner does not believe that applicant believes this is the major feature of this invention, references will only be cited in this action.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,832,031 Hammons, Jr., A. Roger

This patent teaches a method and apparatus for synchronizing and error checking received bitstreams of encoded information. The apparatus includes a single polynomial division shift register. The method involves calculating successive syndromes using the single polynomial division shift register by shifting the received bits of information, generating a syndrome, and comparing the syndrome to a known marker syndrome.

5,636,208 A Chang et al.

This patent teaches a technique for simultaneously performing bit synchronization and error detection of received digital data bursts in a time division multiplexed/time division multiple access (TDM/TDMA) system, such as that used in conjunction with low power portable digital telephony. With the improved technique both bit synchronization and error detection are performed simultaneously to thereby reduce latency in the transceiver.

US 5,502,728 Smith, III, Thomas B.

This patent teaches error correction disabled as a result of detecting an error.

US 4,646,312 Goldsbury et al.

This patent teaches error correction and/or detection disabled as a result of detecting an error.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2138